

PHOTOMASK

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Enabling process window improvement at 45nm and 32nm with freeform DOE illumination

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ABSTRACT

We present a method for optimizing a free-form illuminator implemented using a diffractive optical element (DOE). The method, which co-optimizes the source and mask taking entire images of circuit clips into account, improves the common process-window and 2-D image fidelity. We compare process-windows for optimized standard and free-form DOE illuminations for arrays and random placements of contact holes at the 45 nm and 32 nm nodes. Source-mask cooptimization leads to a better-performing source compared to source-only optimization. We quantify the effect of typical DOE manufacturing defects on lithography performance in terms of NILS and common process-window.

1. Introduction

One of the factors that control the resolution and process window of the lithographic process is how the photomask is illuminated. Off-axis illumination (OAI) is commonly used to improve the resolution and the process latitude. However, there isn't a unique illumination pattern that is applicable to all pat-

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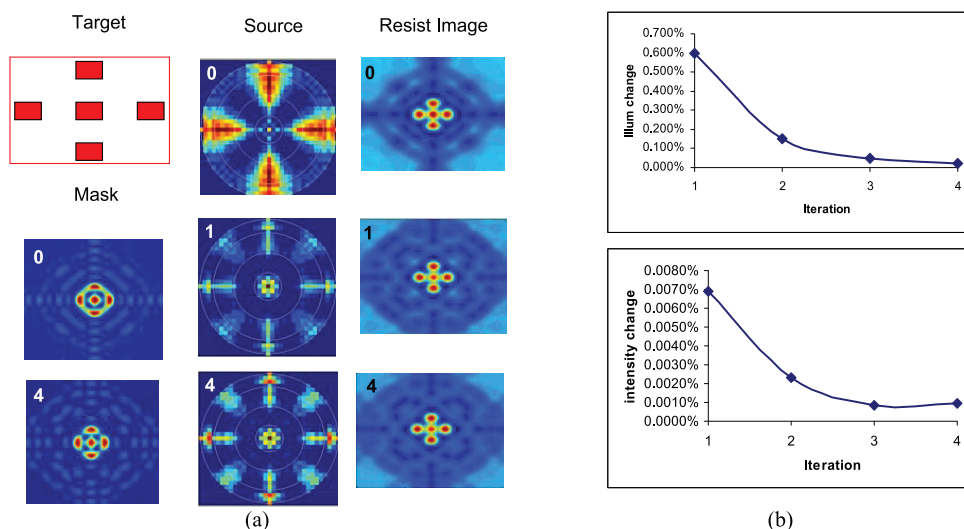


Figure 1. (a) Source, mask and intensity evolution during optimization. (b) Convergence of source and wafer image. The method optimizes the source for multiple layout clips. Only one clip is used in this example for simplicity. The mask images shown here represent the near-field the mask would produce, excluding some high spatial-frequency components, were the mask illuminated with an axial plane-wave.

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SPIE

EDITORIAL

No time to relax!

Ute Buttgercit, Carl Zeiss SMS GmbH

SPIE Advanced Lithography in San Jose has just finished, and although EUV has a made a lot of progress, it became clear that it will not be ready for high-volume production before 2011. Furthermore, it was emphasised that there will be no hyper-NA scanners available, as the development of high-index lens material has been stopped. This means that the industry will stay with 1.35NA scanners for the next technology nodes. Lithographers are forced to print at lower k1, which leads to shrinking process windows and makes getting to high lithographic yield more challenging than ever before.

Double exposure/double patterning and computational lithography like inverse lithography or Source Mask Optimisation (SMO) become the technologies of choice for technology nodes below 45 nm. Clever design layout, design splitting and complex OPC need to be handled, making Design for Manufacturability (DFM) more important than ever. The mission is to reduce design variety, but also to identify hot spots and to reduce design-introduced defects. Computational lithography especially leads to complex mask designs and realises a pixel-based mask optimisation for printing with improved contrast. Source mask optimisation adapts mask design and illumination at the same time, which leads to complex illumination schemes.

Mask data volume and therefore e-beam writing time increase and need to be well controlled. With feature sizes going well beyond the lithography wavelength, the mask becomes more and more of a yield-determining optical element in the printing process, and its performance needs to be precisely qualified. Besides imaging effects caused by the available scanner NA and pitch dependency, 3D mask topography and polarisation will play a major role in the final printing performance and impact the available process window. Additionally, lithography at low k1 increases the Mask Error Enhancement Factor (MEEF) dramatically. Small process variations on the mask will be highly amplified on the wafer print.

These trends make mask process control extremely important. It is no longer sufficient to characterize the geometrical shape of the mask features precisely. This holds true for CD and image placement, but is also required for phase shift measurement. Especially for computational lithography, phase shift provides an additional degree of freedom to enhance the contrast and to control the printing behavior. All imaging-related effects need to be measured, understood, and controlled, which forces the metrology to move to in-die measurements.

For optical metrology, actinic measurement becomes a primary requirement. CD control will become extremely challenging for computational lithography, with a large number and high complexity of sub-resolution assist features needing to be handled, as mask design gets complex and the main features cannot be easily recognized. A possible way out is to quantify the mask performance under scanner conditions. This requires an actinic metrology system with high-quality optics and also with high flexibility in illumination.

In addition to mask process control, repair strategies need to be further developed. Tolerable defect sizes will shrink as well, which requires a repair technology that accounts for the steadily decreasing defect size. Besides dark defects, clear defects also need to be repaired, which requires a precise deposition process and accounting for geometrical and optical requirements, especially for phase shift defects.

It is only a small area that I have covered in this message, but it shows that there is no time to relax. The bar has been raised and it will be a challenging road to the next technology nodes.



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terns. Even for simple patterns, determination of the opening angles and inner and outer radii of the poles requires solving an optimization problem for each set of patterns and process parameters. Simultaneously printing complicated patterns is a more challenging optimization problem which cannot be solved by superposing solutions to simple patterns. Furthermore, the optimum illumination pattern and proximity corrections and assist features are interdependent. This requires an illumination optimization method that jointly optimizes the illumination pattern and mask data.

Most prior work optimizes the source shape for a single periodic pattern, such as the unit cell of a DRAM. This approach has limited practical utility because a chip usually has more than one type of hot-spot or critical pattern. To eliminate this drawback, recent studies¹⁻⁸ considered optimization of the source over multiple patterns as well as mutual optimization of illumination and mask patterns. Most methods optimize metrics such as CD, CD based process windows, and image slope. Methods that seek edge-related goals may fail at other locations such as side-lobes. CD-based metrics also require an initial illumination⁶ which provides sufficient contrast to form the feature and calculate its CD.

The method presented in this paper optimizes the illumination source without requiring an initial illumination. The optimization goals include 2-D image fidelity, edge-placement, image-slope, and depth of focus for multiple layout clips. The method takes into account RET/OPC, mask manufacturability rules, polarization pattern in the pupil, Jones matrix of the projection lens, optical parameters of the resist stack, and resist diffusion.

This method is applicable to both standard and free-form illumination patterns. Most standard and freeform illumination patterns are implemented using diffractive optical elements (DOE, see Figure 3). In practice, a DOE will be used to approximate the optimized illumination. However, given the manufacturing constraints, a DOE will almost always deviate slightly from the intended goal. The variations in the illumination source shape due to DOE manufacturing are estimated and the effect of these deviations on the wafer pattern is quantified. The actual benefit of free-form illumination sources over standard illumination sources can be judged based on this estimate.

In the following sections, we discuss: our source mask optimization method; the performance of freeform illumination and its effect on OPC; the process-window advantage of the free-form DOE over optimal standard illumination; effects of typical variations in the manufacturing of DOEs in terms of NILS and common process-window. We discuss these points by way of case studies of contact-hole layouts for the 45 and 32 nm nodes.

2. Source mask optimization

We present a rapidly-converging method that iteratively optimizes one illumination pattern for multiple layout clips. The method takes into account the entire 2-D image of each layout clip through focus, and it does not require the user to supply an initial guess for the illumination.

Figure 1 shows the convergence of source and mask for a single clip with five rectangular contact holes (smallest dimension is 60 nm). The space between these contacts is 60 nm and this group of contacts is isolated. We assumed a 193 nm dry tool with 0.93 NA. The attenuated phase-shift mask has 6% background transmission and 180° background phase. The results show that the optimization

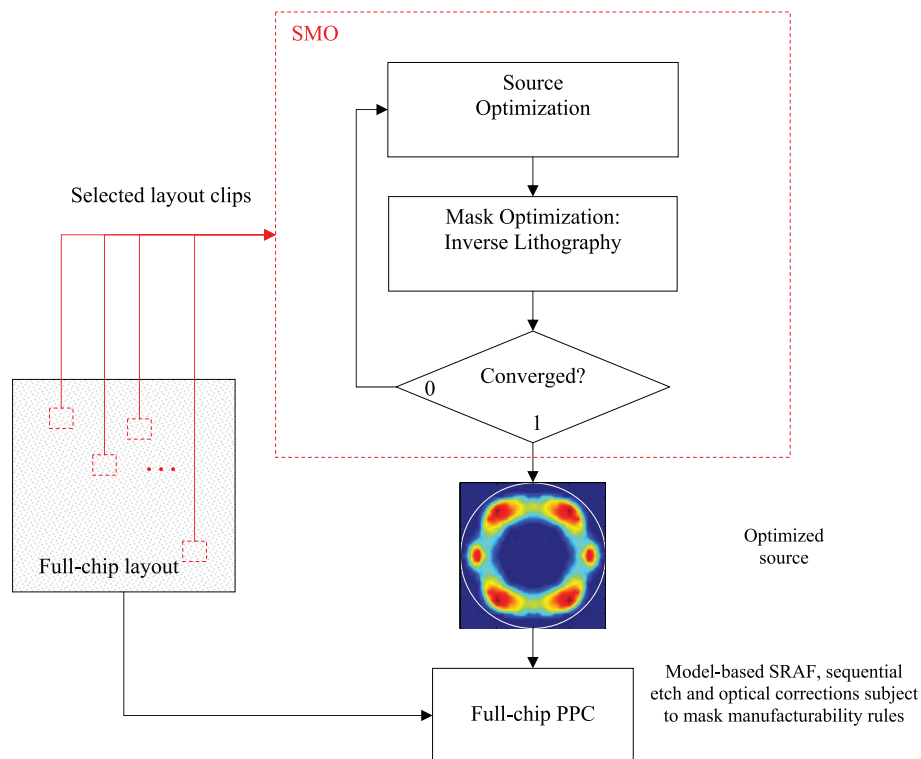


Figure 2. Flow chart for SMO and its use with full-chip process and proximity compensation (PPC).

converged after three iterations with less than 0.05% source and 0.005% intensity changes with respect to previous iterations. The method takes resist blur, variations in focus, and exposure tool characteristics such as polarization and aberration into account. When the illumination pattern is being optimized, usually an RET/OPC recipe is not present. One of the reasons for this is that sub-resolution assist feature (SRAF) placement and illumination are interdependent. Our method eliminates an initial OPC/RET recipe requirement by using inverse lithography in SMO. The optimized mask is constrained to be similar to a selected mask technology, such as an attenuated-PSM mask.¹¹ The mask for the entire chip is subsequently optimized using process proximity compensation (PPC)¹⁴ which includes sequential etch and optical compensations subject to mask-rule constraints. The flow of the overall algorithm is illustrated by Figure 2. This procedure yields a manufacturable illuminator and a manufacturable full-chip mask. Illumination can be restricted to standard shapes or it can have an arbitrary pattern.

3. Diffractive Optical Elements

Diffractive optical elements (DOEs) are widely used as a compact and optically efficient means of controlling the intensity distribution in the pupil plane of a projection illumination system. One of the advantages of using DOEs for controlling the intensity distribution is the variety of patterns that can be realized, from simple dipoles or quadrupoles to the most complex freeform illuminations with multiple intensity variations (see Figure 3). To realize these functions, an iterative design algorithm is used to determine the optimum phase surface of the DOE. The optimized phase surface is quantized to 2^n discrete phase levels (where n is the number of photo/etch levels) and transferred to a reticle. The DOEs are then fabricated on transparent substrates using customized pattern and etch techniques. The difference between the targeted and manufactured performance in the pupil output has been demonstrated to be quite small even for complex patterns.¹⁰ The projected impact

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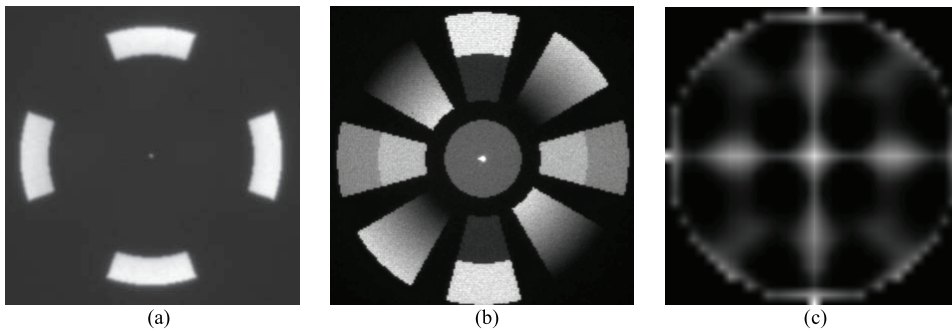


Figure 3. Examples of off-axis pupil illuminations implemented by diffractive optical elements. The intensity distributions (a) and (b) are measured and (c) is simulated.

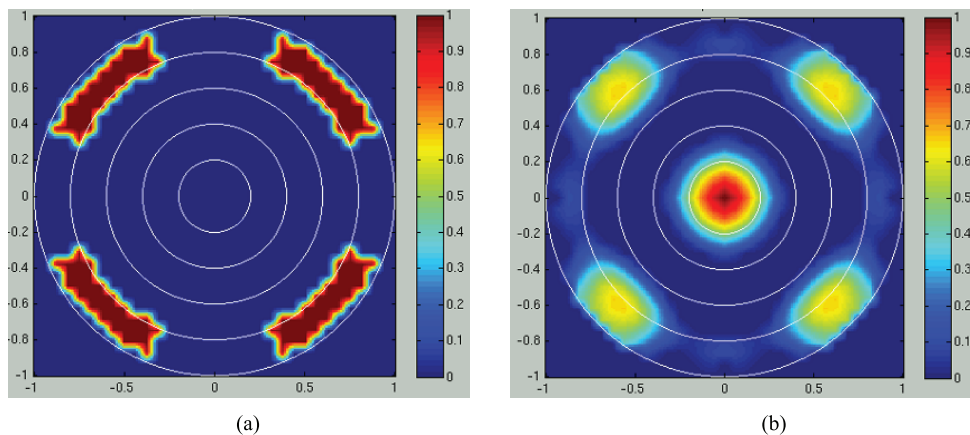


Figure 4. Results of source-mask optimization (SMO) for 2-D square grid of contact holes with pitches between 145 nm and 500 nm. (a) The optimal standard illumination is quadrupole illumination with 0.77 inner and 0.97 outer sigmas. (b) Optimal freeform illumination.

of these differences on the process window for 32nm contact holes is examined in section 4.3.

4. Results

The contact layer has become the lithographically most challenging layer in many sub-45 nm node designs. Particularly difficult contact patterns are randomly placed holes and pitches that make SRAF placement difficult. Therefore, the contact layer is a natural target for source-mask optimization.

4.1 Case study: standard and freeform illuminations for 2-D arrays of contact holes

We study the case of 2-D square arrays of 45 nm contact-holes with 56 nm target CD and pitches ranging from 145 nm to 500 nm. The 193 nm scanner has 1.35 NA. The calibrated litho model contains resist stack information and resist blur. The attenuated PSM has 6% background transmission and 180° background phase.

To establish a base-line performance, we optimize σ_{in} , σ_{out} parameters for annular illumination over nine clips, each clip containing a 2-D array of holes with a different pitch. We use source-only optimization (SO) for the base-line annular illumination. Optimum annular illumination parameters are $\sigma_{in}=0.70$ and $\sigma_{out}=0.97$.

We apply source-mask optimization (SMO) on the same nine clips. The optimized standard and freeform illuminations are shown in Figure 4. The best standard illumination pattern was searched over conventional, annular, bull's eye, quadrupole, C-quad, x-dipole, y-dipole illumination patterns, and their adjustable parameters, subject to the constraints: $0.33 \leq \sigma_{in}$ and $\sigma_{in}+0.2 \leq \sigma_{out} \leq 0.97$. The opening angle for each pole was fixed at 45°. The optimum standard illumination is

quadrupole illumination with $\sigma_{in}=0.77$ and $\sigma_{out}=0.97$. The freeform illumination contains a central pole and a quadrupole of lower intensity.

Figure 5 shows NILS through-pitch for the 2-D square arrays of contact hole after source-mask optimization and applying model-based SRAFs and PPC to the mask polygons. Standard illumination optimized with source-mask cooptimization (SMO) performs better than optimal annular source (SO). Optimal freeform illumination obtained by SMO provides further improvement in NILS.

Figure 6 compares the CD error (the difference between target CD and wafer CD) for optimized standard and freeform illuminations at 50 nm defocus. The through-pitch curves show the advantage of freeform illumination which was already indicated by NILS through-pitch curves.¹¹⁻¹² Among all optimized sources, the standard illumination as obtained from source-optimization-only (SO) shows a lower overall NILS through pitch. This shows that source-mask co-optimization further improves the process window. Figure 6 also supports this where CD Error is the largest from SO optimized illumination.

Figure 7 shows the mask polygons after model-based SRAFs and PPC are applied. The source is optimized for nine pitches but only four pitches are shown for clarity.

4.2 Case Study: Optimum illumination for randomly placed contact holes

In this section, we compare the performances of optimal standard and freeform illumination patterns for randomly placed, 32 nm node contact-holes shown in Figure 8 (a). Such patterns are commonly used in logic devices and in the periphery of memory devices. The minimum pitch of the contact design is 100 nm and the target CD is 55 nm. The 193 nm scanner has 1.35 NA. The calibrated litho model contains resist stack information and resist blur. The attenuated phase-shift mask has 6% background transmission and 180 degree background phase. The free-form illumination pattern optimized by SMO is shown in Figure 8(b). The DOE that implements this pattern was manufactured and its illumination pattern was measured.

To quantify the benefit of the freeform illumination, we also apply source mask optimization to standard source shapes. The optimum standard source shape for this contact pattern is quadrupole illumination with $\sigma_{in}=0.56$ and $\sigma_{out}=0.76$. Figure 9 shows process-window bands for optimized standard, free-form, and fabricated free-form illumination sources. The bands are created by contouring the resist images at $\pm 2\%$ dose and at best focus and 50 nm out of focus. Mask polygons after application of SRAF and OPC are also shown in this figure. The same mask polygons were used for the cases of designed and manufactured free-form illuminations. Naturally, OPC/SRAF was applied separately for the optimal standard illumination according to its imaging model. Figure 10 shows the normalized intensities along cutline C1 from standard and freeform illuminations. The image contrast is higher for the freeform illumination than for the optimal standard illumination. The contrast of the images increased from 23%/20% (best

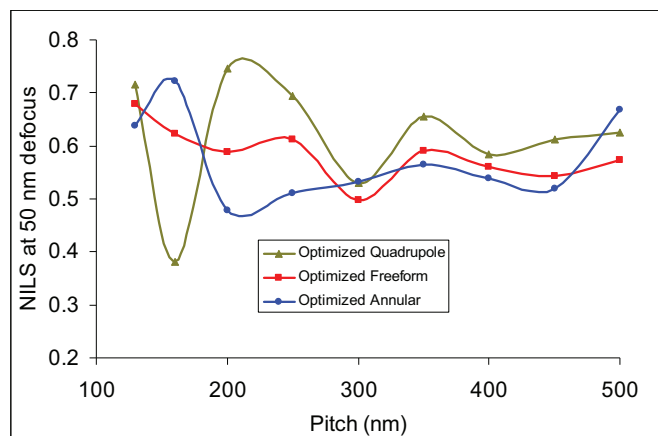


Figure 5. NILS through pitch for 2-D square arrays of contact holes at 50 nm defocus. Quadrupole and free-form illumination patterns have been optimized by source-mask optimization. Annular illumination pattern has been optimized by source optimization. Model-based SRAFs and OPC have been applied to mask polygons.

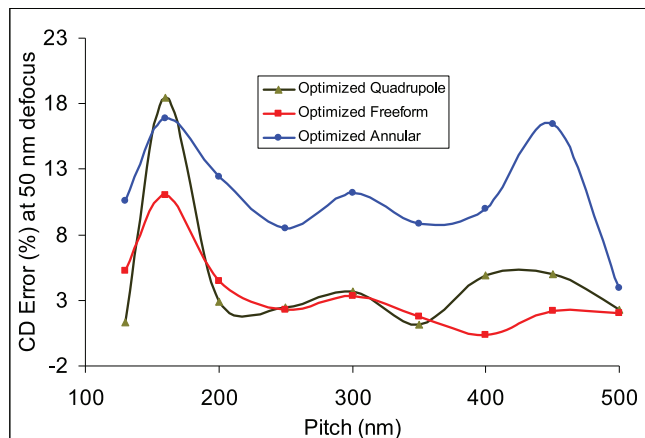


Figure 6. CD Error (%) through-pitch at 50 nm defocus, for quadrupole, annular, and freeform illuminations. Model-based SRAF and PPC were applied to the polygons using the respective imaging models.

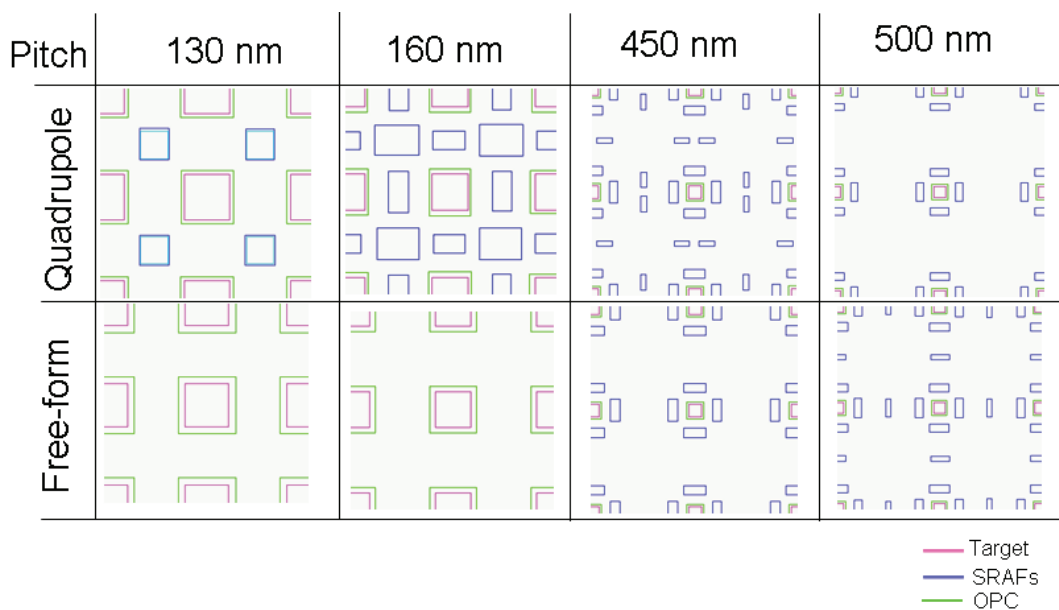


Figure 7. Mask polygons after model-based SRAFs and PPC are applied following optimization of the standard and freeform sources. The optimal standard illumination was a quadrupole. Mask polygons were generally simpler for the freeform source in this example.

focus/50 nm defocus) to 30%/37%. Figure 11 shows the common process windows for optimized standard illumination and designed versus actual manufactured freeform illuminations. The depth of focus (DOF) is 40 nm at 4% Exposure Latitude (EL) for standard illumination while it is 95 nm for freeform illumination. This reflects over 100% improvement in DOF for the same exposure latitude. Figure 12 gives the NILS for each cutline at best focus and 50 nm defocus for freeform and standard illuminations. The NILS remained the same or improved at all cutline locations. The largest improvement occurred at the location with the lowest NILS (C2).

4.3 DOE manufacturing effects

In this section we examine how DOE manufacturing affects the performance of freeform illumination for the design discussed in Section 4.2.

We fabricated the optimized freeform illumination by using Tessler's DOE technology and measured its intensity profile. Figure 13 shows the designed and measured intensity maps and their difference. The difference between the designed and measured source maps is RMS 0.59% and maximum 1.24% of the peak of the designed source map. We run simulations by using the fabricated DOE illumination to calculate the common process window. In this analysis, the same mask polygons (SRAF/PPC output) obtained for the designed freeform illumination are also used for the measured freeform illumination.

Figure 11 compares the process-windows for the designed and measured freeform sources. DOE manufacturing limitations account for 8 nm reduction in depth of focus (DOF) and 1% reduction in expo-

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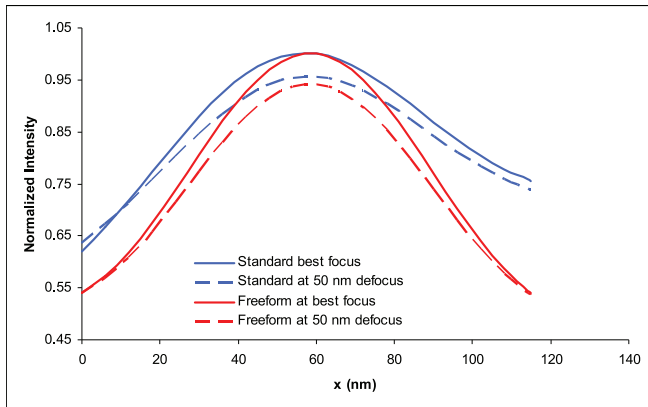
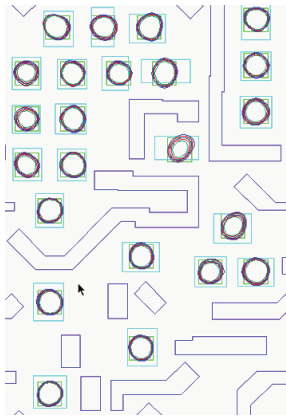
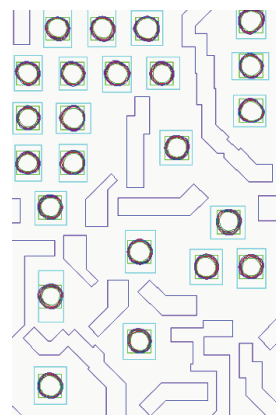


Figure 8. (a) A contact test design and (b) corresponding optimum free-form illumination.



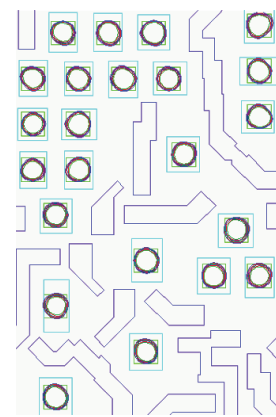
(a)

Optimal standard source



(b)

Optimal freeform source



(c)

Actual manufactured freeform source

Figure 9. Process-window bands for optimized (a) standard (b) free-form, and (c) actual fabricated free-form illumination sources for the layout shown in Figure 8. Model-based SRAFs and OPC were applied to case (a) and (b) using imaging models for the respective illuminations. The same mask polygons were used in (b) and (c).

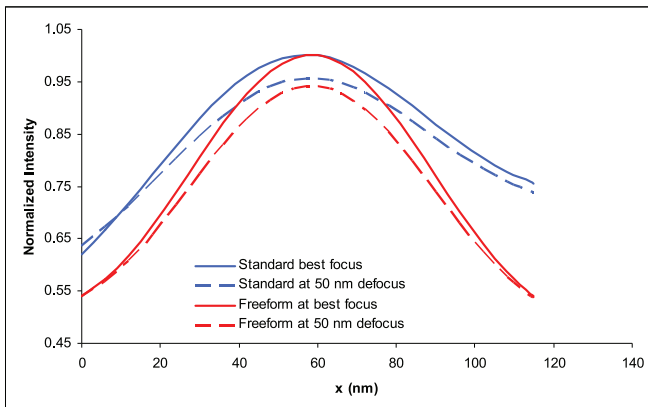


Figure 10. Normalized intensity profiles for cutline C1 in Figure 8(a) for: the optimized freeform source as designed (Freeform); and the optimized standard source (Standard).

sure latitude (EL) at best focus. These losses are small compared to the gains achieved by using a freeform source over the best standard source, as can be seen in Figure 11.

In this analysis, standard illuminations are assumed to have ideal top-hat shapes. In reality, standard illuminations are not ideal and they are also generated by DOEs that are subject to similar manufacturing effects.¹³

5. Conclusions

We demonstrated a method for optimizing the illumination source for multiple layout clips. The method, which is applicable to optimizing standard illumination options or a freeform illumination, is based on resist images calculated taking exposure tool characteristics and process conditions into account. Optimal freeform illumination performed better than the optimal standard illumination in case studies of 2-D arrays and random placements of contact holes at the 45 and 32 nm nodes. Freeform illumination provided higher image slope and lower out-of-focus CD error compared to the best standard illumination.

We fabricated the optimized freeform illumination by using Tessler's DOE technology and measured its intensity profile. The measured source map deviated from the designed source map by RMS 0.59% of the peak of the designed source map. The process-window loss due to the source error was small compared to the gain offered by the freeform source for the specific contact-hole layout we studied.

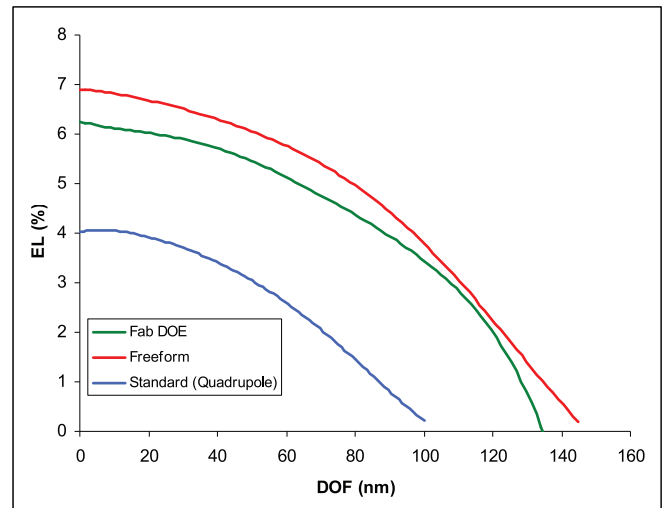


Figure 11. Common process windows for: the optimized freeform source as designed (Freeform); the freeform source as fabricated (Fab); and the optimized standard source (Standard).

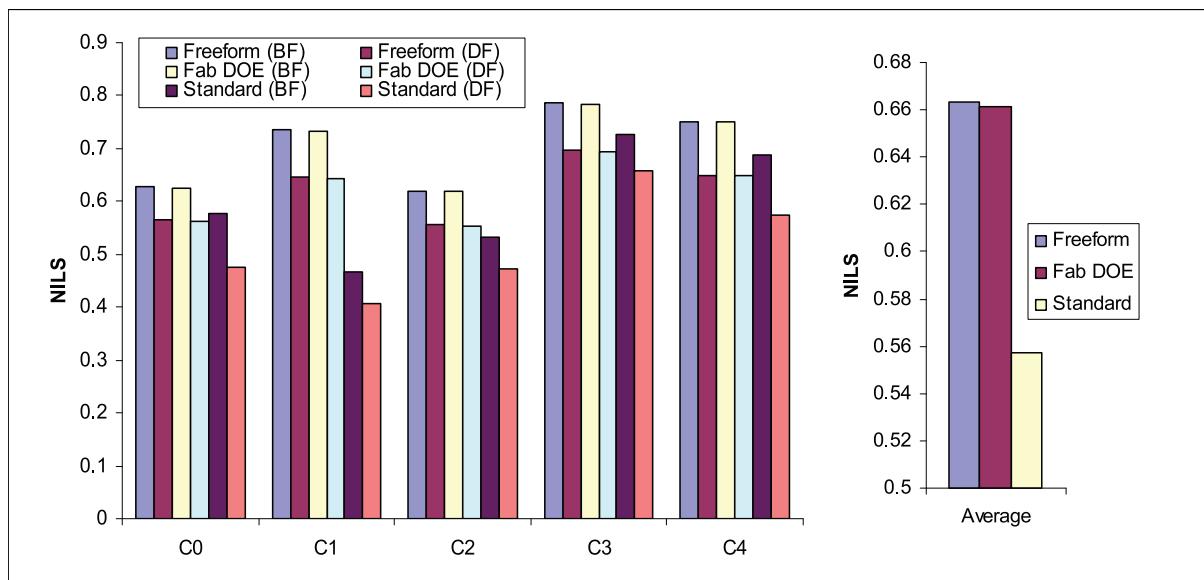


Figure 12. NILS at the cutlines shown in Figure 8(a) at best focus (BF) and 50 nm out of focus (DF) for: optimum standard illumination (Standard); freeform illumination as designed (Freeform); and freeform illumination as fabricated (Fab DOE).

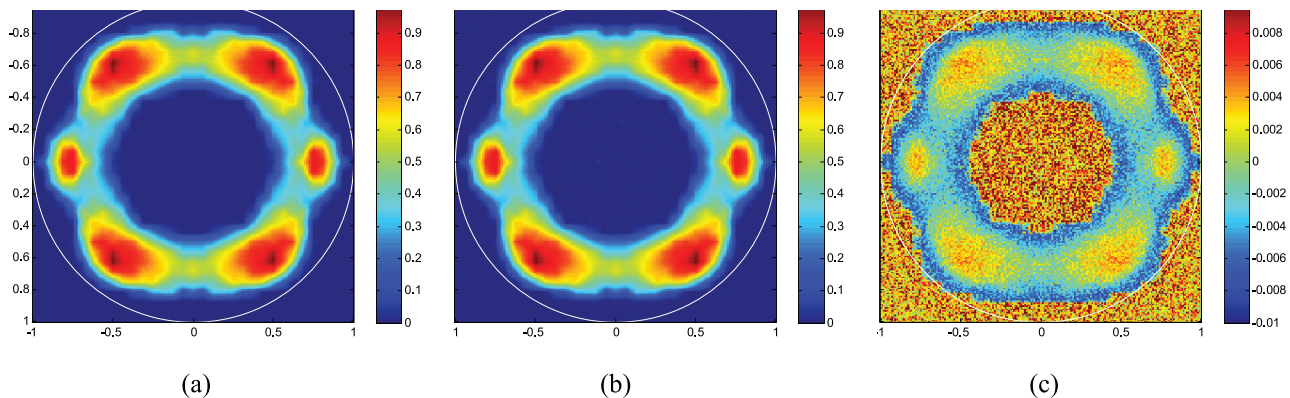


Figure 13. (a) Optimized DOE source (b) Manufactured and measured DOE source (c) Difference between designed and measured intensity patterns. Note that the range of the color axis is $[0, 1]$ for (a) and (b) but $[-0.01, 0.01]$ for the difference (c).

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Industry Briefs

■ SPIE Observations: EUV vs. "All Other" Litho

By **Ken Rygler**, Rygler & Assoc. and Molecular Imprints

SPIE is considering splitting the Alternative Lithography Technologies into two conferences: EUV and "all others". Motivation seems twofold — EUV papers continue to increase, while SPIE is looking to "all others" as a means to draw in more applications, such as hard disk drives, flat-panels, solar, biotech, and perhaps others. These seem to be reasonable goals, but there is cost. The industry has made a huge investment in EUV. Its history has been checkered, and that is being gracious: two steps forward and one step back, with the net effect of delaying market entry for many years (some would say: too many years). Renaming "SXPL" (soft x-ray projection lithography) to the more marketable "EUV" did not change the wavelength, or the fact that it is X-ray lithography which has always been fraught with a daunting list of challenges, any one of which can keep a number of engineers, scientists, academics, and students busy for years. And while an endless flow of papers is assured, a commercial success is not.

"All other" lithography technologies have drawn new applications into SPIE's predominantly semiconductor lithography conference. For example, the hard disk industry has always been involved, given their optical patterning of thin-film read/write heads. Hard disks are now moving to patterned media, and will deploy imprint technology to pattern over one billion disks, more than the global consumption of 8-inch equivalent silicon wafers. Attendance by members of the hard disk industry has increased as a consequence, as has their submission of papers.

Recently, imprint has emerged as a serious challenger to EUV, particularly in the high-volume non-volatile memory dominated by NAND flash. While two alpha EUV tools have been sold to IMPLSE and IMEC, two step-and-flash imprint lithography beta tools have been sold to Toshiba and SEMATECH. Recent cost-of-ownership data has given imprint a significant edge vs. both EUV and optical double patterning. In addition, e-beam direct write (aka ML2, aka maskless) is enjoying somewhat of a renaissance, thanks to at least one foundry promoting its use in small wafer runs. If SPIE does indeed split the current Alternative Lithography Technology Conference into two conferences, SPIE must manage it in a way that lithography managers will not be faced with impossible choices when scheduling their time.

■ Source-Mask Optimization Continues on Track

By **Alexander E. Braun**, Semiconductor International

IBM (Hopewell Junction, N.Y.) and Mentor Graphics (Wilsonville, Ore.) announced an initiative to develop source-mask optimization(SMO) in time for the 22 nm node, a move in part prompted by the slow development of EUV lithography. SMO would enable the pixel-level programming of illumination sources and the extension of 193 nm immersion lithography for 22 nm, and is expected to reduce manufacturing costs while improving turnaround by improving process windows (dose, focus, mask error). SMO is being developed like no another OPC product ever was, by a globally integrated team. At the SPIE Advanced Lithography in San Jose, representatives from IBM and Mentor Graphics said they are currently transitioning code from the research prototype into Mentor's Calibre design-to-silicon. "Every two nodes, we end up trying to find a new way for resolution enhancement to overcome the gap in k_1 , that the hardware companies cannot provide," said Charles Albertalli, marketing director at Mentor. "So, until we get to EUV, 193 it is and the NA is 1.35, and that doesn't seem as if it's going to change. At 65, 45 nm, we went from sparse to dense OPC. Now, at 22 nm, dense OPC isn't enough; we need to take advantage of every degree of freedom in the optical system and in the capabilities in software development to minimize the application of double patterning, which obviously has significant cost implications."

At this point, SMO is the way to go, although it is no simple undertaking. One reason is that it is computationally intensive. But as Albertalli put it, "Fortunately, with IBM, we have a resource to develop onto the most advanced hardware platforms." Timothy Farrell, manager of IBM's Computational Lithography Group, emphasized that EUV will not be available in time for 22 nm, pointing out that the additional benefits derived from 193 nm immersion lithography have flattened at 32 nm. There's no new inherent resolution capability, but it is going to be possible to cut the amount of double exposure levels by 20-35%. "It also looks like we will be able to reduce design constraints in moving to 22 nm and working in a low k_1 environment. At the same time, it enables the setting up of a platform extendable to 16 nm, which will have to use double exposure." By that time, this will be a mature technology. And by then — perhaps — the industry will not still be waiting for EUV.

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